--Notice: More than one reissue application has been filed for the reissue of Patent No. 5,811,318. The present reissue application is a continuation of reissue application no. 09/667,663, which is a reissue of Patent No. 5,811,318.--

In the claims:

Please amend the following claims with the same claim numbers as follows.

1. (Amended) A method for manufacturing a liquid crystal display, comprising the steps of:

forming a gate electrode and a gate pad by depositing a first metal film and a second metal film over a substrate in a TFT area and a gate-pad connecting area, respectively, by a first photolithography process;

forming an insulated[ing] film over the gate electrode and the gate pad;

forming a semiconductor film pattern over the insulated[ing] film in the TFT area by a second photolithography process;

forming a source electrode/drain electrode and pad electrode in the TFT portion and the pad portion, respectively, using a third photolithography process, the source electrode/drain electrode and the pad electrode all being comprised of a third metal film;

forming a passivation film pattern [by a fourth photolithography process, the passivation film] exposing a portion of the drain electrode, a portion of the gate pad, and a portion of the pad electrode, and etching the insulated film over the portion of the gate pad, by a fourth photolithography process;

exposing the first metal film by etching a portion of the second metal film that comprises the gate pad using the passivation film pattern as a mask; and

forming a first pixel electrode pattern connected to the drain electrode of the TFT area [by a fifth photolithography process, the pixel electrode acting to connect the gate pad of the gate-pad connecting area to the pad electrode of the pad area] and a second pixel electrode pattern acting to connect the gate pad of the gate-pad connecting area to the pad electrode of the pad area using a fifth photolithography process.

8. (Amended) A method for manufacturing a liquid crystal display, comprising steps of:

forming a gate electrode and a gate pad by depositing a first metal film and a second metal film over a substrate in a TFT area and a pad area, respectively, by a first photolithography process;

forming an insulated film over the gate electrode and the gate pad;

forming a semiconductor film pattern over the insulated[ing] film in the TFT area by a second photolithography process;

forming a source electrode and a drain electrode in the TFT area by a third photolithography process, the source electrode and the drain electrode comprising a third metal film;

forming a passivation film pattern that exposes a portion of the drain electrode on the TFT area and a portion of the gate pad of the pad area by forming a passivation

film over the source electrode and the drain electrode and performing a fourth photolithography process on the passivation film and the insulated film;

exposing the first metal film of the pad area by etching the second metal film using the passivation film pattern as a mask; and

forming a first pixel electrode pattern that is connected to the drain electrode of the TFT area [and contacts] and a second pixel electrode pattern that is connected to the first metal film of the pad area by a fifth photolithography process.

Please add the following new claims:

16. A TFT substrate, comprising:

a gate electrode comprising a first metal film over a substrate and a second metal film over the first metal film;

a gate pad consisting the first metal film and a portion of a removed area of the second metal film;

an insulated film over the gate electrode and having an exposed area of the first metal film over the gate pad;

a semiconductor film pattern over the insulated film;

a source electrode formed over a first portion of the semiconductor film pattern;

a drain electrode formed over a second portion of the semiconductor film pattern;

a passivation film pattern formed over the source electrode, having a contact hole over the drain electrode and having an exposed area of the first metal film of the gate pad;

a first pixel electrode pattern electrically contacted to the drain electrode on the passivation film pattern; and

a second pixel electrode pattern electrically contacted to the exposed area of the first metal film of the gate pad.

17. A TFT substrate, as recited in claim 16, wherein the first metal film comprises a refractory metal.

18. A TFT substrate, as recited in claim 17, wherein the first metal film comprises a material selected from the group consisting of CR, Ta, Mo, and Ti.

19. A TFT substrate, as recited in claim 16, wherein the second metal film comprises A1 or an A1 alloy.

20. A TFT substrate, as recited in claim 16, wherein the insulated film comprises a nitride film SiN.

21. A TFT substrate, as recited in claim 16, wherein the first and second pixel patterns comprise ITO.

22. A TFT substrate, as recited in claim 16, wherein a portion of the passivation film directly contacts the semiconductor film pattern.

23. A TFT substrate, comprising:

a gate electrode comprising at least a refractory metal film formed over a first portion of a substrate;

a gate pad comprising the refractory metal film formed on a second portion of a substrate;

an insulated film formed over the gate electrode and having an exposed area corresponding to the refractory metal film of the gate pad;

a semiconductor film pattern formed over the insulated film;

a source electrode formed over a first portion of the semiconductor film pattern;

a drain electrode formed over a second portion of the semiconductor film pattern;

a passivation film pattern formed over the source electrode, having a contact hole over the drain electrode and having an exposed area corresponding to the refractory metal film of the gate pad;

a first pixel electrode pattern electrically contacted to the drain electrode on the passivation film pattern; and

a second pixel electrode electrically contacted to the exposed area of the refractory metal film of the gate pad.

24. A TFT substrate, as recited in claim 23, wherein the refractory metal film comprises a material selected from the group consisting of Cr, Ta, Mo, and Ti.

25. A TFT substrate, as recited in claim 23, further comprising a second metal film formed on the refractory metal film over the first portion of the substrate, and formed on the refractory metal film of the gate pad except for the exposed area thereof.

26. A TFT substrate, as recited in claim 23, wherein the second metal film comprises A1 or A1 alloy.

27. A TFT substrate, as recited in claim 23, wherein the insulated film comprises a nitride film SiN.

28. A TFT substrate, as recited in claim 23, wherein the first and second pixel patterns comprise ITO.

29. A TFT substrate, as recited in claim 16, wherein a portion of the passivation film directly contacts the semiconductor film pattern.

30. A method for manufacturing a liquid crystal display as in claim 1, wherein the gate electrode is formed so that at least one of the first and the second metal film has tapered-sidewalls.

31. A method for manufacturing a liquid crystal display as in claim 30, wherein the second metal film has tapered sidewalls.

32. A method for manufacturing a liquid display as in claim 1, wherein forming the semiconductor film pattern comprises:

forming an amorphous silicon film on the insulated film;

forming a doped amorphous silicon film on the amorphous silicon film; and

patterning the doped amorphous silicon film and the amorphous silicon film.

33. A method for manufacturing a liquid crystal display as in claim 1, wherein the second pixel electrode pattern contacts portions of the exposed gate pad.

34. A method for manufacturing a liquid crystal display as in claim 8, wherein the gate electrode is formed so that at least one of the first and the second metal film has tapered-sidewalls.

35. A method for manufacturing a liquid crystal display as in claim 34, wherein the second metal film has tapered sidewalls.

36. A method for manufacturing a liquid crystal display as in claim 8, wherein forming the semiconductor film pattern comprises:

forming an amorphous silicon film on the insulated film;

forming a doped amorphous silicon film on the amorphous silicon film; and

patterning the doped amorphous silicon film and the amorphous silicon film.

37. A method for manufacturing a liquid crystal display as in claim 8, wherein the second pixel electrode pattern contacts portions of the exposed gate pad.

38. A TFT substrate as in claim 16, wherein at least one of the first and the second metal film of the gate electrode and the gate pad has tapered-sidewalls.

39. A TFT substrate as in claim 38, wherein the second metal film has tapered sidewalls.

40. A TFT substrate as in claim 16, wherein the semiconductor film pattern comprises:

an amorphous silicon film on the insulated film; and

a doped amorphous silicon film on the amorphous silicon film.

41. A TFT substrate as in claim 16, wherein the second pixel electrode pattern contacts portions of the exposed gate pad.

42. A TFT substrate as in claim 23, wherein at least one of the first and the second metal film of the gate electrode and the gate pad has tapered-sidewalls.

43. A TFT substrate as in claim 42, wherein the second metal film has tapered sidewalls.

44. A TFT substrate as in claim 23, wherein the semiconductor film pattern comprises:

an amorphous silicon film on the insulated film; and

a doped amorphous silicon film on the amorphous silicon film.

45. A TFT substrate as recite in claim 23, wherein the second pixel electrode pattern contacts portions of the exposed gate pad.

46. A TFT substrate, comprising:

a substrate;

a gate electrode and a gate line formed over the substrate, having a metal film with tapered sidewalls;

a gate pad formed over the substrate, contacted to an end portion of the gate line;

an insulating film formed over the gate electrode, having a hole which exposes the gate pad;

a semiconductor film pattern formed over the insulated film including the gate electrode, having an amorphous silicon and a doped amorphous silicon;

a source electrode formed over the semiconductor film pattern;

a drain electrode formed over the semiconductor film pattern;

a data line formed over the semiconductor film pattern, connected to the source electrode;

a passivation film pattern formed over the source electrode, having a first and a second hole, wherein the first hole exposes the drain electrode and the second hole exposes a portion of the gate pad;

a first pixel electrode pattern formed over the passivation film, contacted to the exposed drain electrode; and

a second pixel electrode pattern contacted to the exposed portion of the gate pad.

47. A TFT substrate as in claim 46, wherein a portion of the passivation film directly contacts the semiconductor firm pattern.

48. A TFT substrate as in claim 46, wherein the gate electrode and the gate pad comprise at least a refractory metal film.

49. A TFT substrate as in claim 48, wherein the refractory metal film comprises a material selected from the group consisting of Cr, Ta, Mo, and Ti.